PTO 04-[0676]

Japanese Patent

Sho 58-23091

IMAGE DISPLAY DEVICE

[Gazo Hyoshi Sochi]

Hideo Toyo

UNITED STATES PATENT AND TRADEMARK OFFICE

Washington, D.C. November 2003

Translated by: Schreiber Translations, Inc.

Country	:	Japan
Document No.	:	Sho 58-23091
Document Type	:	Kokai
Language	:	Japanese
Inventor	:	Hideo Toyo
Applicant	:	Daini Seikosha K.K.
IPC	:	G 02 G 3/36, G 02 F 1/133, G 09 F 9/35
Application Date	:	August 4, 1981
Publication Date	:	February 10, 1983
Foreign Language Title	:	Gazo Hyoshi Sochi
English Title	:	IMAGE DISPLAY DEVICE

Specification

1. Title of the invention

Image Display Device

2. Claims

1. An image display device, characterized by the fact that in an image display device in which picture element electrodes are formed in a matrix shape on a semiconductor layer formed on an insulating substrate such as glass or on a semiconductor substrate and transparent electrodes on a light-transmitting substrate installed via a liquid crystal on the above-mentioned image electrodes are opposite electrodes, at least one switching element and a 1-bit memory cell are provided for one of the above-mentioned picture element electrodes; and the output of the above-mentioned memory cell and the picture element electrodes are connected.

2. An image display device, characterized by the fact that in an image display device in which picture element electrodes are formed in a matrix shape on a semiconductor layer

[1] Numbers in the margin indicate pagination in the foreign text.

formed on an insulating substrate such as glass or on a semiconductor substrate and transparent electrodes on a light-transmitting substrate installed via a liquid crystal on the above-mentioned image electrodes are opposite electrodes, at least one switching element, a one-bit memory cell, and a signal selecting circuit in which each phase is inverted when the output of the above-mentioned memory cell is at "H" level and "L" level are provided for one of the above-mentioned picture element electrodes; and the output of the above-mentioned signal selecting circuit and the picture element electrodes are connected.

3. <u>Detailed explanation of the invention</u>

The present invention pertains to a fine dot image display device using a liquid crystal without requiring a half tone.

A conventional image display device is shown in Figure 1. It is constituted by combining a liquid crystal and a MOS type FET array. In Figure 1, a unit picture element consists of MOS type FET 1a formed on a semiconductor layer, capacitor 2a for storing signals, and liquid crystal cell 3a. Its basic operation is explained. First, if the MOS type FET is used as a P channel and a negative pulse voltage as a gate signal is applied to a gate line F1, the FET 1a is turned on, and an image

signal added to the signal line F1 is charged in the capacitor 2a through the FET 1a. If the negative pulse disappears, the FET 1a is turned off, and the voltage charged in the capacitor/2 is held while being discharged through the liquid crystal cell. Then, the gate signal is linearly scanned from X_i to X_{i+1} and X_{i+2}, and image signals corresponding tot eh positions are added from Y_i, Y_{i+1}, etc., so that the entire image is displayed. At that time, the opposite electrodes are transparent electrodes attached to the entire surface by glass, etc., and a COM of Figure 1 is a common electrode terminal. Then, the common electrode is always held at a certain potential. On the other hand, such an image display device was appropriate for the case where analogue signals or dynamic images were displayed, that is, for displaying television images, however it was very inappropriate for displaying images without requiring a half tone and still images. The reason for this is that since the signal charged in the capacitor 2a is discharged through the liquid crystal cell 3a as mentioned above, even if a high-level signal "1" is written as shown by a by a curve 4 of Figure 2, the voltage at the rear end of the capacitor 2a is almost lowered until the next writing, so that the writing operation is always required for a period Ta, even for the case where static images are displayed, thereby always requiring a power for

moving the entire circuit. Similarly, a curve S shows the voltage at the rear end of the capacitor 2a. Furthermore, the increase of the power consumption due to the repetition of the charge and discharge to the capacitor could not be avoided.

Accordingly, the purpose of the present invention is to provide an image display device with low power consumption suitable for displaying images without requiring a half tone and still images.

Next, the present invention is explained along with the figures. Figure 5 shows the image display device of the present invention. A unit picture element consists of MOS type FET 6a formed on a semiconductor layer, 1-bit memory cell 7a, and liquid crystal cell 8a. Here, in the memory cell 7a, if "1" signal is input, the output is set to "1" ("0"), and the initial state is held until "0" signal is input. If "0" signal is input, the output is set to "0" ("1"), and this state is held. If the image display device with this constitution is used, as shown in Figure 6, if write pulses X_i and X_{i+1} are applied for a certain time and information "1" is written into the memory cell from Y_i and Y_{i+1}, the information "1" is continuously applied to the liquid crystal for a long term until the next write pulse is applied and "0" information is newly written.

Therefore, if the voltage level of "1" and "0" and the voltage level of the common electrode are determined so that a selective voltage may be applied to the liquid crystal at "1" and a nonselective voltage may be applied to the liquid crystal at "0," images without a half tone and its still images can be displayed at a very low power. The reason for this is that driving circuits of signal lines Y_i, Y_{i+1}, etc., and the gate lines X_i, X_{i+1}, etc., can be stopped in still images. Also, the reason for this is that signals are not charged in the capacity and the output voltage of the memory cell is controlled basically without sending a current. Also, 9 and 10 of figure 4 show the output voltage of each memory cell 7a and 7b.

Figure 5 shows a detailed application example of the memory cell part of the image display device of the present invention. In other words, input and output terminals of CMOS inverters 12 and 13 are connected to each other, the input of the inverter 12 is connected as an input of the memory cell to a switching transistor 11, and the output of the inverter 13 is connected as an output of the memory cell to [illegible] voltage.

Figure 6 shows another image display device of the present invention. In the example of Figure 6, an alternating-current driving function is further provided and consists of a switching transistor, that is, MOS FET 11, CMOS inverters 12 and 13,

liquid crystal cell 14, EXCLUSIVE OR circuit 15, and clock source 16. The constitution of the memory cells of the CMOS inverters 12 and 13 is similar to that of the example of Figure 5. However, the output of the memory cell is connected to one input terminal of the EXCLUSIVE OR circuit (hereinafter, abbreviated to EOR circuit) 15, and the other input terminal of the EOR circuit 15 and the common electrode terminal CMO are connected. Furthermore, a clock for an alternating-current driving is input into the common electrode terminal. In the case where the output of the memory cell is "1" and "0," the voltage being applied to the liquid crystal is respectively shown in Figures 7 and 8. First, if the output of the memory cell is "1," an inverted signal 16a at a waveform 17 of the /3
clock source is obtained as an output of the EOR circuit 15. Accordingly, if the output of the EOR circuit 15 is connected to the picture element power source, as shown in 19a of Figure 7, an alternating-current driving waveform of ± V voltage is applied to the liquid crystal. Next, if the output of the memory cell is "0," a signal 160 with the same phase as that the waveform 117 of the clock source is obtained as an output of the EOR circuit 15. Thus, no voltage is applied to the liquid crystal. Therefore, when the input is "1," a selective alternating-current voltage is applied to the liquid crystal,

and when the input is "0," no voltage is applied to the liquid crystal. Since the driving is always carried out by an alternating current, the long life and the reliability of the liquid crystal can be improved. Figure 9 further shows another application example of the image display device of the present invention. It consists of switching transistor 11, CMOS inverters 12 and 13, transmission gates (hereinafter, abbreviated to TG) 20 and 21, liquid crystal cell 14, and clock source 16. The constitution of the memory cell of the CMOS inverters 12 and 13 is similar to that of the example of Figure 5. However, the output of the memory cell, that is, the output of the CMOS inverter 13 is connected to a n channel side gate of the TG 20 and a P channel side gate of the TG 21, and the input terminal of the CMOS inverter 13 is connected to a P channel side gate of the TG 20 and a n channel side gate of the TG 21. Then, the outputs of the TGs 20 and 21 are connected to each other as a picture element power source, and the input terminal of the TG 21 is connected with a common electrode and connected with the clock source 16. Furthermore, the input terminal of the TG 20 is connected to the clock source 16 via an inverter 24. With this constitution, when the output of the memory cell is "1," the TG 209 is turned on, and the TG 21 is turned off. Thus, an alternating-current driving waveform of the same ± V as

that of 19a of Figure 7 is applied to the liquid crystal cell. Similarly, when the output of the memory cell is "0," no voltage is applied to the liquid crystal cell. The example of Figure 9 is favorable for a high densification of the picture elements since the number of picture elements for creating the circuit is smaller than that of the example of Figure 6. Also, in the examples of Figures 6 and 9, the alternating-current driving is made possible by the EOR circuit and the TGs. In other words, this operation can be achieved by any circuit that can invert the polarity of the clock being applied to the picture element power source when the output of the memory cell is "1" and "0." In addition to the example using the EOR circuit and the TGs, a similar operation can also be realized by the combination of an EXCLUSIVE NOR circuit and an AND circuit and the combination of an OR circuit, and needless to say, they can also be included in the range of the present invention. Also, the circuit constitution in which a selective voltage is applied when the input signal is "0,"is similar, and its explanation is omitted. Also, in the examples of Figures 6 and 9, in the still image display, the clock source is [illegible], and the peripheral circuits are stopped similarly to the examples of Figure 3 and 5.

With the use of the image display device of the present invention with the above constitutions, the image display device with the intended purpose, that is, the image display device which is suitable for displaying images without requiring a half tone and its still images at a low power consumption can be achieved. In other words, the entire circuit constitutional is digitalized, and all the peripheral circuits are stopped to display still images. Thus, a large power consumption reduction can be realized. Also, since an alternating-current driving is possible, an excellent display device in terms of lifetime and reliability can be obtained. Therefore, with the application of the present invention to character display devices such as characters and graphics, a beautiful display of [illegible] dots, a low power consumption, and a long life and high reliability can be simultaneously achieved. Therefore, the industrial values of the present invention are great.

4. <u>Brief description of the figures</u>

Figure 1 is a circuit diagram showing a conventional image display device.

Figure 2 is an illustrative diagram showing the relationship between a write pulse and a liquid crystal driving voltage in Figure 1.

Figure 3 is a circuit diagram showing an application example of the image display device of the present invention.

Figure 4 is an illustrative diagram showing the relationship between a write pulse and a liquid crystal driving voltage in Figure 3.

Figure 5 is a circuit diagram showing a detailed application example of the image display device of the present invention.

Figure 6 is a circuit diagram showing another application example of the image display device of the present invention.

Figures 7 and 8 are illustrative diagrams showing the liquid crystal driving voltage in Figure 6. /4

Figure 9 is a circuit diagram showing another application example of the image display device of the present invention.

6a, 6b, 11	Switching elements
7a, 7b	Memory cells
8a, 8b, 3a	Liquid crystal cells
9, 10	Liquid crystal driving voltages
12, 13	CMOS inverters
15	EXCLUSIVE OR circuit
16	Clock source
17	Clock waveform
16a	Selective clock

16b	Nonselective clock
19a	Selective driving voltage
19b	Nonselective driving voltage
20, 21	Transmission gates
22	Clock input terminal and common electrode terminal
23	Driving clock input terminal
24	Inverter

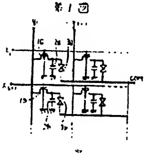

Figure 1

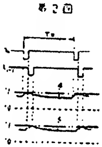

Figure 2

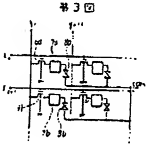

Figure 3

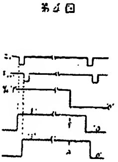

Figure 4

第5図

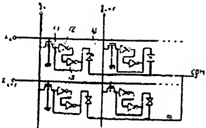

Figure 5

第7図

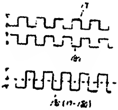

Figure 7

第8図

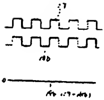

Figure 8

第6図

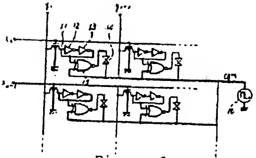

Figure 6

第9図

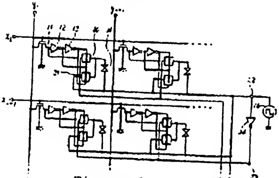

Figure 9